

### General Description

The AO6602 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications.

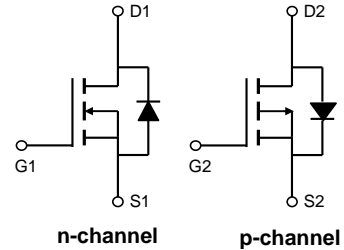
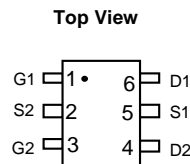
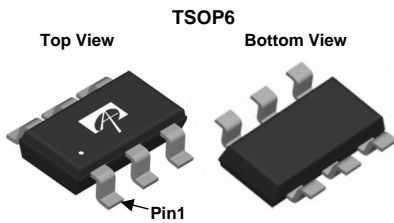
### Product Summary

#### N-Channel

$V_{DS} = 30V$   
 $I_D = 3.5A$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 50m\Omega$  ( $V_{GS} = 10V$ )  
 $< 70m\Omega$  ( $V_{GS} = 4.5V$ )

#### P-Channel

$-30V$   
 $-2.7A$  ( $V_{GS} = -10V$ )  
 $R_{DS(ON)} < 100m\Omega$  ( $V_{GS} = -10V$ )  
 $< 170m\Omega$  ( $V_{GS} = -4.5V$ )



### Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	-2.7	A
		$T_A = 70^\circ C$	-2.1	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	20	-15	
Power Dissipation <sup>B</sup>	$P_D$	$T_A = 25^\circ C$	1.15	W
		$T_A = 70^\circ C$	0.73	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	78	110	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>				
Maximum Junction-to-Lead	$R_{\theta JL}$	64	80	$^\circ C/W$

**N-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.5	2	2.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	20			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A T <sub>J</sub> =125°C		40 61	50 77	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A		52	70	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =3.5A		12		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.79	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				1.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		170	210	pF
C <sub>oss</sub>	Output Capacitance			35		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			23		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.7	3.5	5.3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =3.5A		4.05	5	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			2	3	nC
Q <sub>gs</sub>	Gate Source Charge			0.55		nC
Q <sub>gd</sub>	Gate Drain Charge			1		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =4.2Ω, R <sub>GEN</sub> =3Ω		4.5		ns
t <sub>r</sub>	Turn-On Rise Time			1.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			18.5		ns
t <sub>f</sub>	Turn-Off Fall Time			15.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =3.5A, dI/dt=100A/μs		7.5	10	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =3.5A, dI/dt=100A/μs		2.5		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

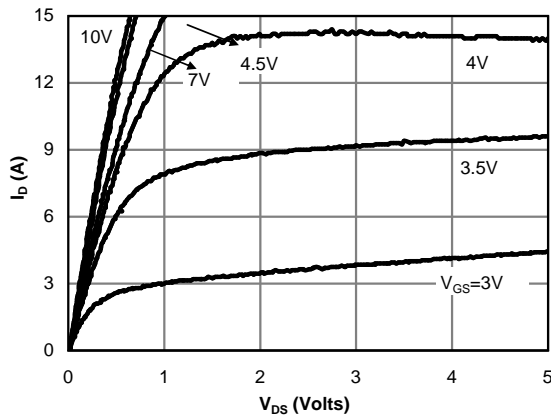
D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

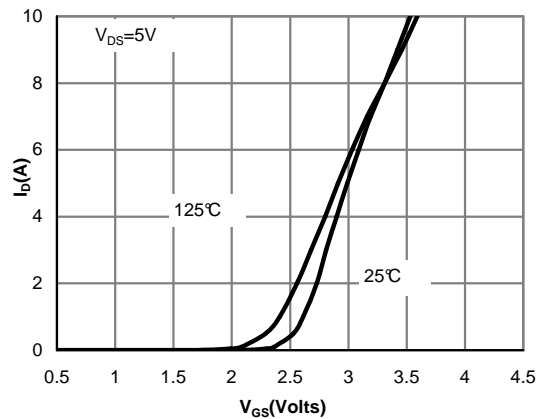
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

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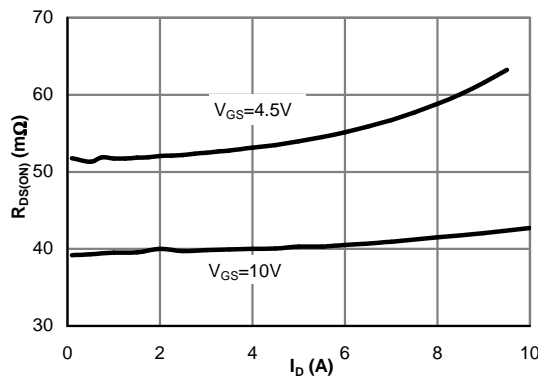
**N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



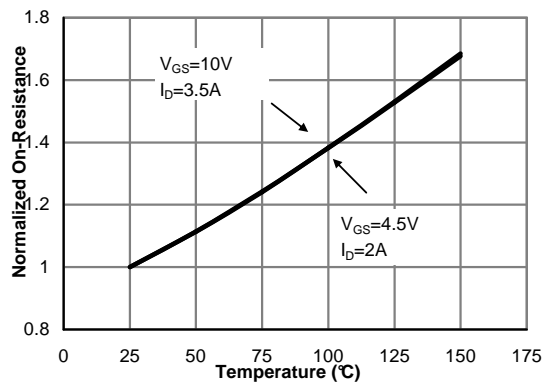
**Figure 1: On-Region Characteristics (Note E)**



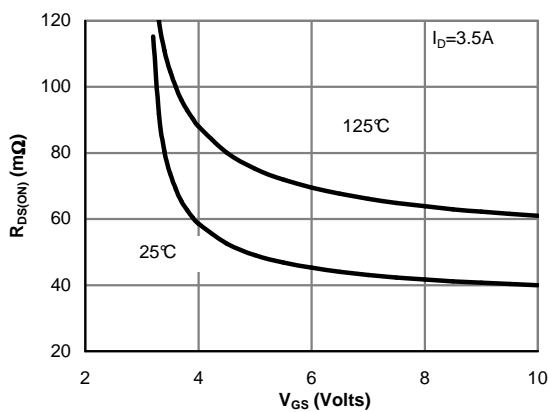
**Figure 2: Transfer Characteristics (Note E)**



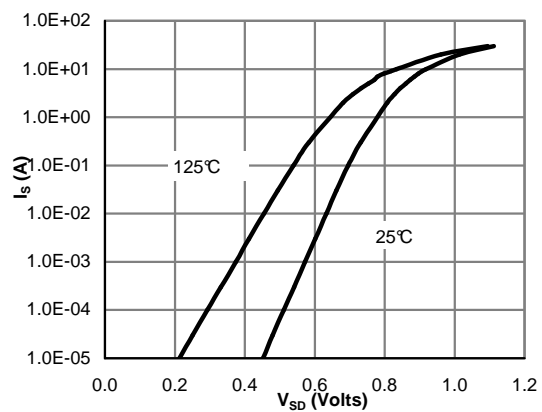
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

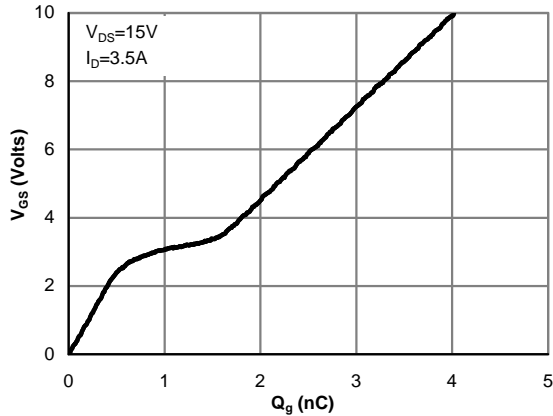


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

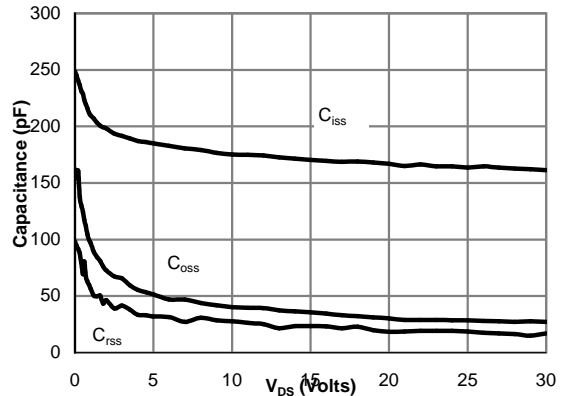


**Figure 6: Body-Diode Characteristics (Note E)**

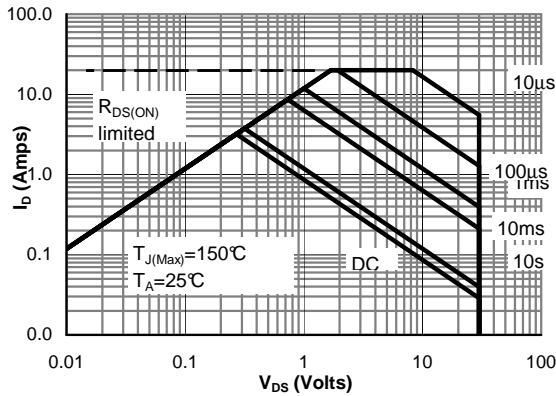
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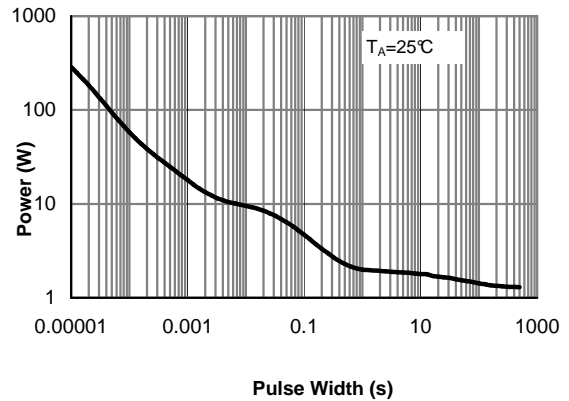
**Figure 7: Gate-Charge Characteristics**



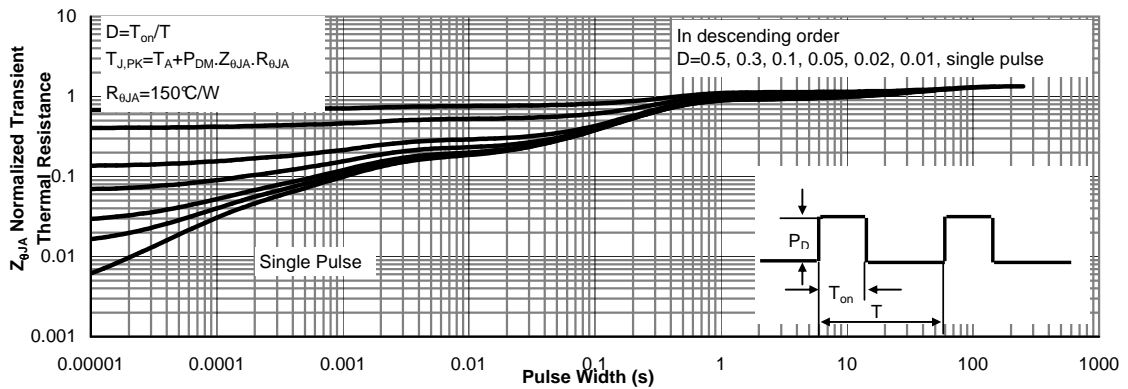
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

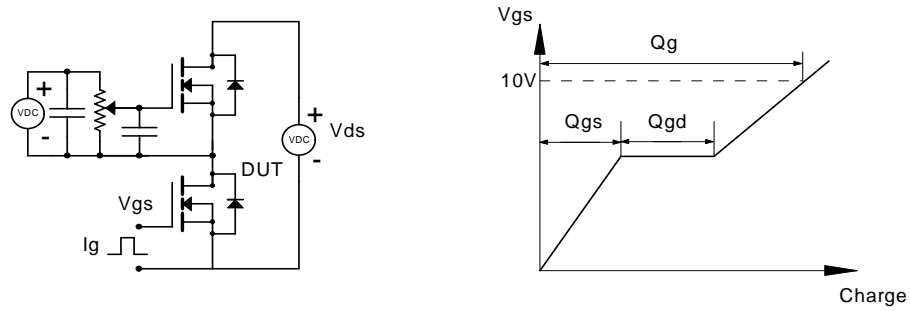


**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

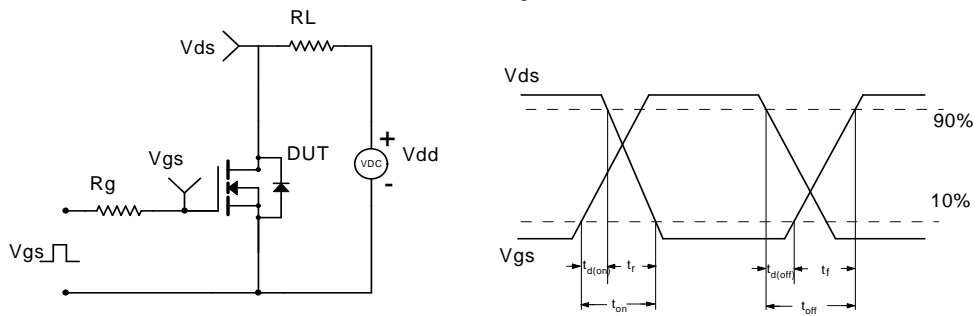


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

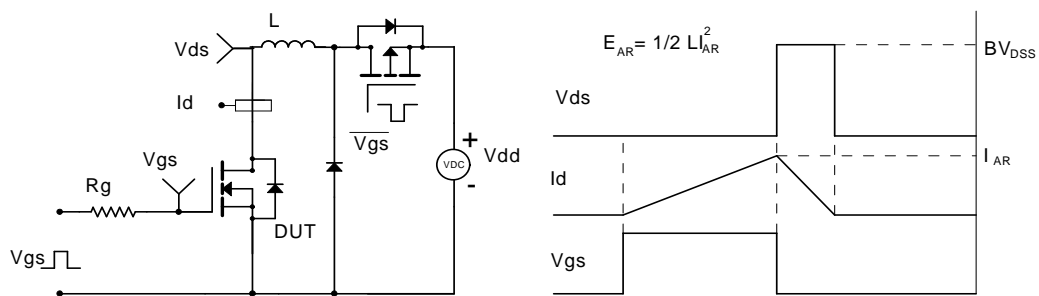
**Gate Charge Test Circuit & Waveform**



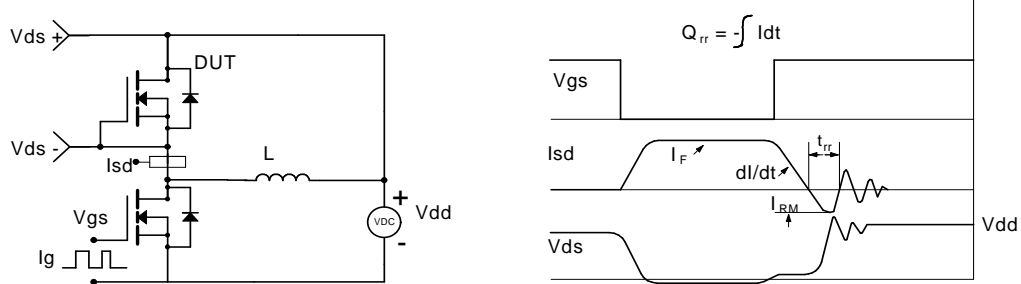
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



P-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$ , $V_{GS}=0\text{V}$	-30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-1.4	-1.9	-2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$ , $V_{DS}=-5\text{V}$	-15			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$ , $I_D=-2.7\text{A}$ $T_J=125^\circ\text{C}$		82	100	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$ , $I_D=-2\text{A}$		115	140	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}$ , $I_D=-2.7\text{A}$		5.5		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}$ , $V_{GS}=0\text{V}$		-0.8	-1	V
$I_S$	Maximum Body-Diode Continuous Current				-1.5	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=-15\text{V}$ , $f=1\text{MHz}$		197	240	pF
$C_{oss}$	Output Capacitance			42		pF
$C_{riss}$	Reverse Transfer Capacitance			26	37	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$	3.5	7.2	11.0	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=-15\text{V}$ , $I_D=2.7\text{A}$		4.3	5.2	nC
$Q_g(4.5\text{V})$	Total Gate Charge			2.2	3	nC
$Q_{gs}$	Gate Source Charge			0.7		nC
$Q_{gd}$	Gate Drain Charge			1.1		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$ , $V_{DS}=-15\text{V}$ , $R_L=5.55\Omega$ , $R_{GEN}=3\Omega$		7.5		ns
$t_r$	Turn-On Rise Time			4.1		ns
$t_{D(off)}$	Turn-Off DelayTime			11.8		ns
$t_f$	Turn-Off Fall Time			3.8		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-2.7\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		11.3	14	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-2.7\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		4.4		nC

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ\text{C}$ , using  $\leq 10\text{s}$  junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

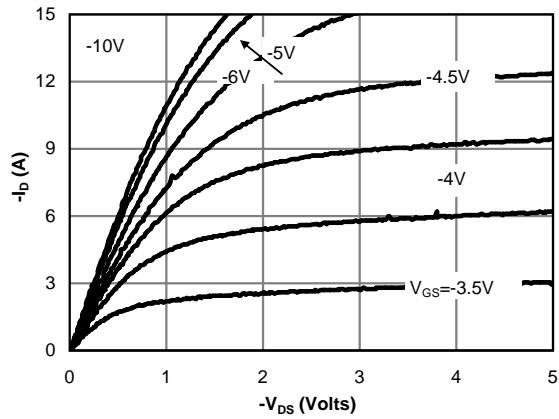
D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

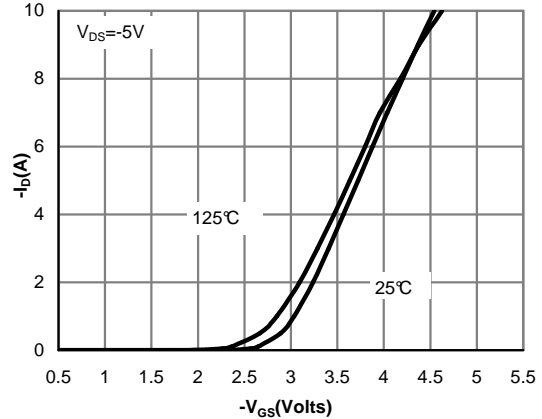
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of  $T_{J(MAX)}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.

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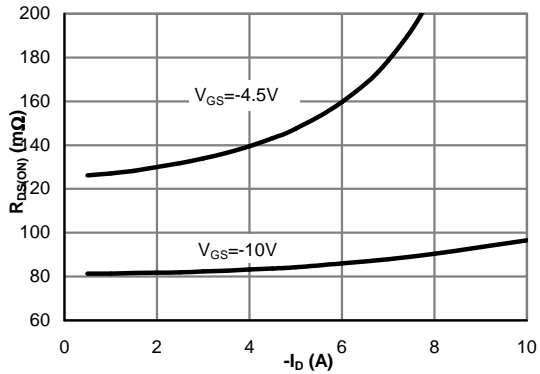
**P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



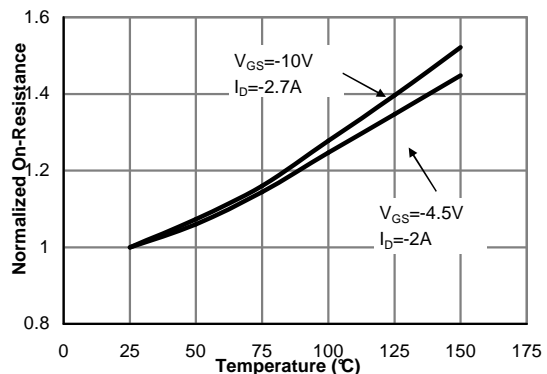
**Figure 1: On-Region Characteristics (Note E)**



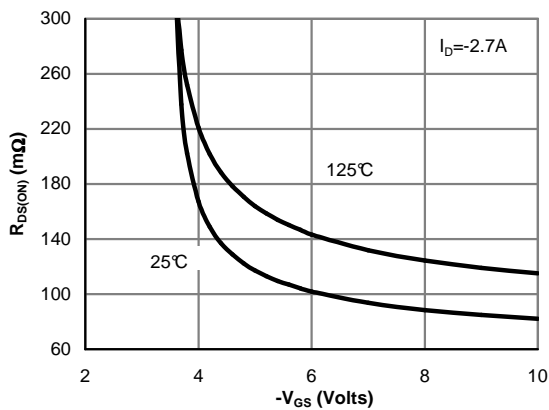
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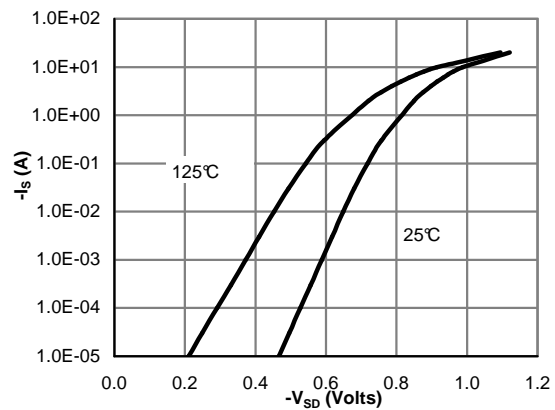
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

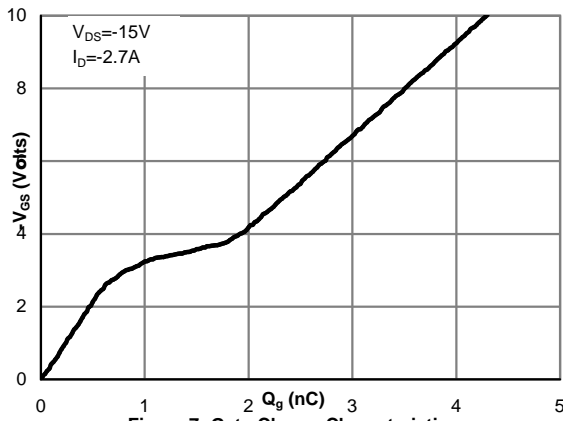


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

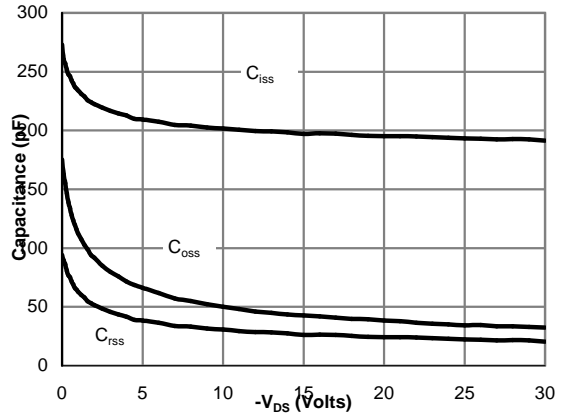


**Figure 6: Body-Diode Characteristics (Note E)**

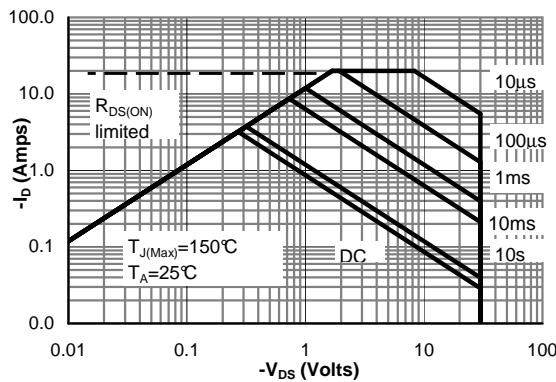
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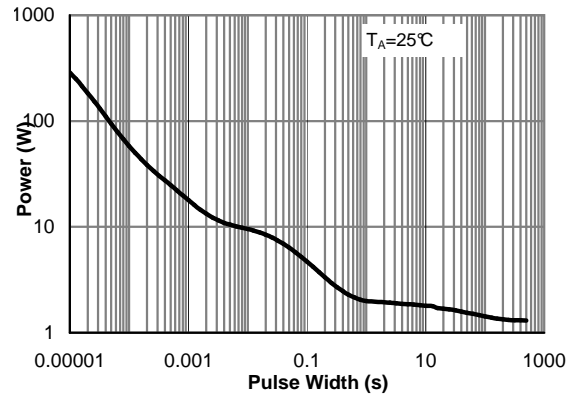
**Figure 7: Gate-Charge Characteristics**



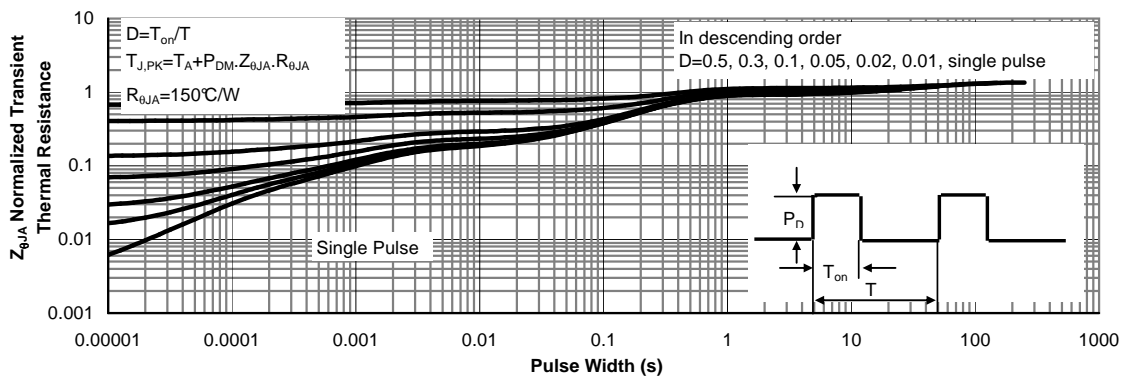
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



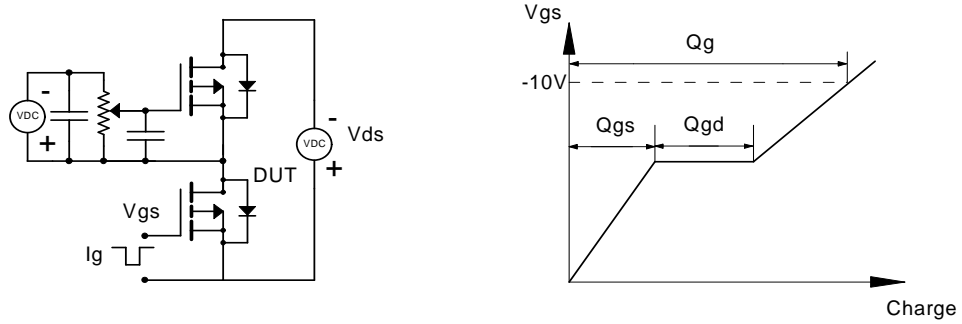
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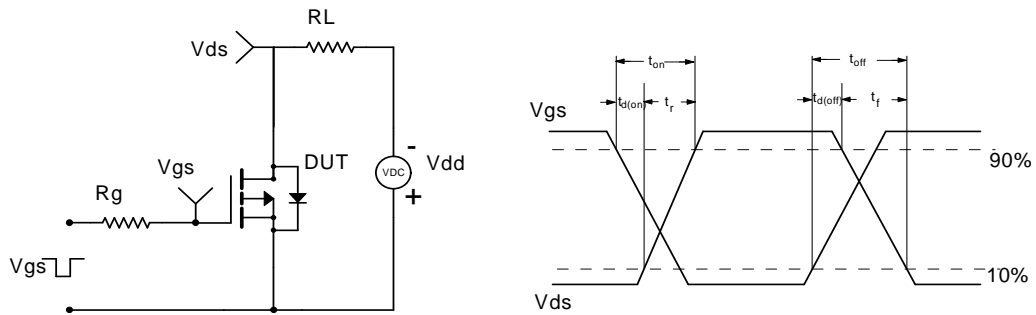
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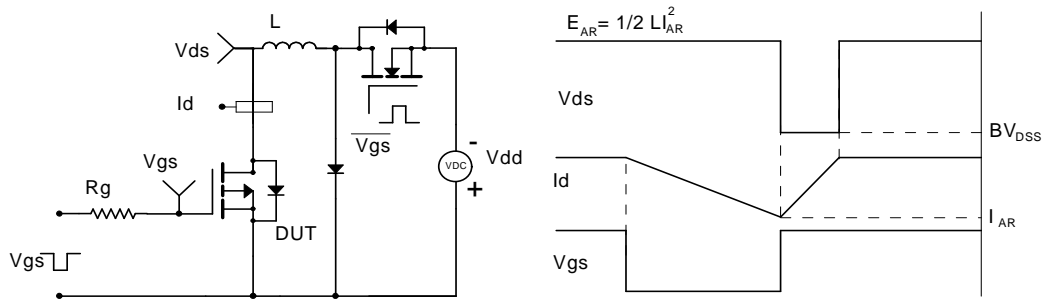
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

